Comprehensive study on fault-ride through and voltage support by wind power generation in AC and DC transmission systems

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Abstract

This paper exploits the impact of different Low Voltage Ride-through (LVRT) methods and equipment on both the wind energy elements and the grid including wind turbine/farm ability to provide reactive compensation, and maintain controllability during faults. The potential of using SFCL as an alternative LVRT equipment is preliminary studied. The paper also exploits some severe scenarios that could face a multi-terminal HVDC network. The influences of AC faults and control errors are examined. Results show limited deviations between the adopted LVRT methods. The wind turbine has to contribute to the stability of the AC collection grid of the wind farm, but it does not influence the grid, as both are decoupled through the multi-terminal HVDC grid. The implemented test systems and the examined events are developed in Matlab/Simulink and DIgSILENT.

1 Introduction

The growing wind energy penetration is enforcing changes to power systems configurations, Grid Codes and dynamics. Hence, it is required to exploit a wide range of scenarios and develop new control methods to ensure grid resiliency. One of the key challenges is voltage stability, and all the incorporated elements to maintain it. This paper navigates through two technologies to transmit wind power: the mature medium/high AC voltage, and the developing multi-terminal high voltage DC grids, which could be a key enabler to the foreseen interconnected Pan-European power system. However, the real-world application of DC grids is exposed to doubts and technical concerns, which requires intensive research efforts to examine different scenarios and provide potential solutions

Power systems are subject to several types of voltage events including 3-phase symmetrical faults of different severity levels based on the fault impedance, single phase-to-phase or phase-to-ground faults, in addition to moderate voltage sags due to sudden changes in generation and/or load demand [1, 2]. The wind turbine generator (WTG) has to protect itself during such events, as low voltage results in high currents and raises the voltage of the DC link in case of Double Fed Induction Generators (DFIG; Type 3) and Permanent Magnet Synchronous Generator (PMSG; Type 4). There are a wide range of protection methods, which aim to suppress the fault current through the WTG, and dissipate the input mechanical energy during voltage events [3]. Moreover, the WTG has to provide reactive compensation to contribute to the recovery of voltage to the standardised safe margin. The entire LVRT process must comply with the applied Grid Code, which is enforced by Transmission System operator (TSO). The compliance is assessed at the Point of Common Coupling (PCC, or Connection Point as an alternative terminology) of the wind farm (WF) to the grid (i.e. not at the connection point of each WTG to the collection network of the WF). Nevertheless, if the WTG is connected directly as an independent generator to the grid, it has to comply with the Grid Code if its rating is above a certain limit defined by TSO [4]. Thus, the main challenge is to protect generation assets, and provide the required reactive compensation. Apart from LVRT hardware, some researchers aimed proposed new control methods to avoid the integration of LVRT hardware [5], but the industry does not widely adopt this approach.

The connection topology of the WTG and the WF are also critical to the applied LVRT techniques, hence this paper exploits two different topologies, conventional AC connectors, and Multi-terminal HVDC grids. The two topologies were widely discussed from the frequency stability perspective in a previous paper [6]. In addition, the paper compares between LVRT methods including the type of measurements to sense faults, connection durations of LVRT hardware. Moreover, a DC grid is examined through a highly detailed model of a key part of the Cigre benchmark. Some modifications are applied to the network, including the replacement of one of the AC grids by an aggregate synchronous generator of equivalent size to exploit its response. The test system rides through some bottlenecks under different control modes to reveal the weaknesses of the generic controls of the DC grid converter stations.

2 Grid Codes common requirements

Grid codes define when the generation unit is allowed to disconnect (i.e. trip) during voltage dips as shown in Figure 1, the unit must keep connected as long as the minimum voltage (V_{fault}) is sustained for a duration shorter than fault clearance time (t_{clear}). The relays of rate of change of voltage are tuned to accommodate the post-fault voltage recovery (t_{clear} to t_{rec1}). The recovery could face an intermediate halt as a low voltage level sustains until t_{rec2}, however, the generator must keep connected within the defined time span. Some TSOs adopt different patterns, for example, the intermediate recovery phase is not included to allow higher tolerance [7, 8].

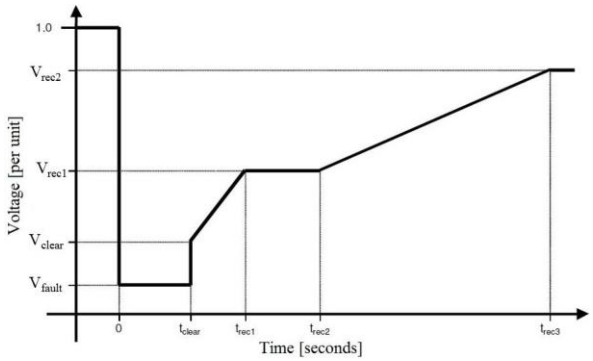


Figure 1. Generic LVRT Grid Code requirements.

Limits	Value	Time	Value
V_{fault}	5 - 30%	t_{clear}	0.14 - 0.25s
V_{clear}	70 – 90%	t_{rec1}	$t_{rec1} \geq t_{clear}$
V_{rec1}	$V_{clear} < V_{rec1} < V_{rec2}$	t_{rec2}	$t_{rec1} < t_{rec2} < 0.7s$
V_{rec2}	85 - 95%	t_{rec3}	$t_{rec2} < t_{rec3} < 1.5s$

Table 1. Reference parameters during frequency events.

The typical values of the pivot voltage and time points of this pattern are in Table 1. This should be the first part of compliance, where the second part is the provision of reactive compensation during voltage recovery to normal margin (i.e. typically 1 ± 0.1 per unit). According to the majority of Grid Codes [9, 10], the generation unit should maintain 1 per unit reactive power/current injection during voltage dips, and then it reduces gradually relying on voltage response. Some Grid Codes define the required pattern of the injected reactive current at different voltage levels, similar to the main ride through curve, however, it is more accurate to define the reactive current rather than the reactive power as the voltage dip mitigates the capability of active power transmission, and hence the value of current is more achievable and critical. Further details on Grid Codes and the development of generic requirements that could be achieved by wind energy systems are found in [11].

3 AC systems

This paper focuses on three hardware: crowbar (with two different topologies: AC or DC circuitry), DC chopper, and SFCL as illustrated in Figure 2. The LVRT capabilities of WTG and its compliance with Grid Codes rely on four key elements, the protection hardware, sensed parameters to trigger/connect the hardware, and its connection as illustrated in Figure 3. The SFCL is designed to act as a superconductor when rotor current is within safe limits.

3.1 Test system and scenarios

The SFCL is located in two different positions, in series between Rotor Side Converter (RSC) and DC-link capacitor, or as a 3-phase component between the induction machine rotor and the RSC. The SFCL is not affected by the applied triggering method of the LVRT, as it changes its conduction status naturally according to the persistent fault current. The i_q and i_d set-points of the RSC controller are adjusted to 0.05 per unit, when the LVRT equipment are active, hence even if the SFCL is deployed, the sensing method will amend the *d* and *q* reference currents during the fault. This should support the RSC to safely ride through the fault.

The test system suffers from 2 consecutive 3-phase faults of the same impedance $0.1+j0.1$ **Ω**, first occurs at B2, and the second occurs at B3 after 1.5s as shown in Figure 2, both faults continue for 150ms. All the scenarios are examined at wind speed of 15 m/s to secure the rated output of the WTG, which is considered as worst-case scenario. The conventional AC crowbar 3-phase connected resistors, and DC crowbar where a 3-phase rectifier connects a limiter resistance during faults relying on the adopted LVRT method. The proposed controllers and scenarios/case studies are integrated and examined into the detailed and highly accredited DFIG model in Simulink®. The simulation time step is 5μs to ensure accurate capturing of the transients of system components. The following two scenarios exploit the impact of the applied event-sensing methods at *a constant connection time of 40ms.*

Scenario 1 *– DC voltage junction sensing*: The performances of the three protection hardware are compared and analysed from the viewpoints of response time and WTG safety. A different protection device is examined separately in the WTG model, under unified fault conditions and connection time, where the DC voltage of the WTG junction is the fault detection signal. In particular, when the DC voltage exceeds 1.02 per unit, the protection hardware is triggered, these thresholds are inspired by the results obtained in [12].

Scenario 2 *– Voltage at PCC sensing*: It is similar to Scenario 1 but the sensing signal is the voltage at PCC, such that when it drops below 0.15 per unit, inspired by some Grid Codes [13] protection device is triggered. The details of applied parameters of LVRT hardware modelling are in Table 2.

Both scenarios are tested for different LVRT hardware as discussed in the next subsection.

3.2 Results and discussion

This section analyses the most relevant results due to the large amount of obtained data for the exploited scenarios.

Voltage response

The voltage at the DFIG and the DC link are brought to focus to investigate the DFIG response during faults. The fault-sensing method has minor impact on the response obtained, this returns to the simultaneous consequences of the event. For example, the voltage across the DC link overshoots at the same instant the rotor current rises above the threshold.

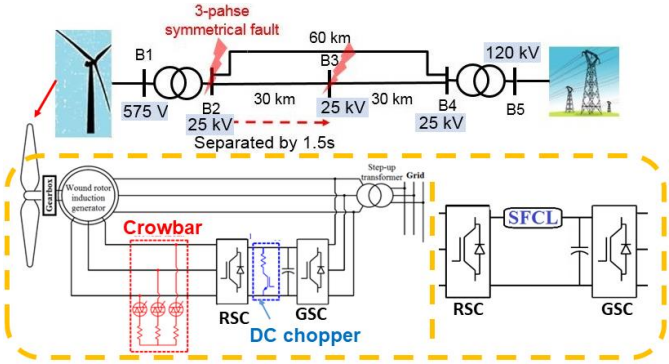


Figure 2. Implemented test system.

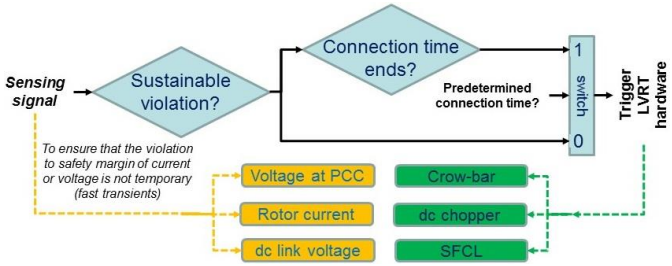


Figure 3. The applied fault detection and LVRT methods.

Equipment parameters		SFCL parameters	
DC chopper resistance	5 Ω	SC diameter	AC: 9.2 mm DC: 10 mm
crowbar resistance	0.1 Ω	SC resistivity	2.57 μΩ.m^2
DC crowbar resistance	0.3 Ω	Efficiency of heat removal	2.5 kW.K/m^2
Sensing delay	1ms	Critical temperature	95 K
Sustainability delay	10ms	Transitory electric field to flow state	0.1 V/m

Table 2. Parameters of LVRT equipment.

In addition, the sensing and sustainability delays dissolve the major divergences between the two examined scenarios as show in Figure 4 (a) and (b). The divergence between the three examined LVRT hardware is also limited on voltage at DFIG bus, however, the overshoot in the DC link is improved when the two topologies of conventional crowbar is applied, meanwhile, no deviation is observed between the other methods, where the 3-arms DC crowbar achieved the lowest overshoot. It is of note, the improved DC link voltage during the second fault as shown in Figure 4(b) since the fault is relocated to Bus 3 with the privilege of the presence of an alternative transmission line. The voltage dip at DFIG is not improved that much, while the PCC voltage is worse and it dropped to 0.6 pu, as the fault moves closer to the grid (PCC voltage response is not shown due to space limits).

Rotor and converter currents

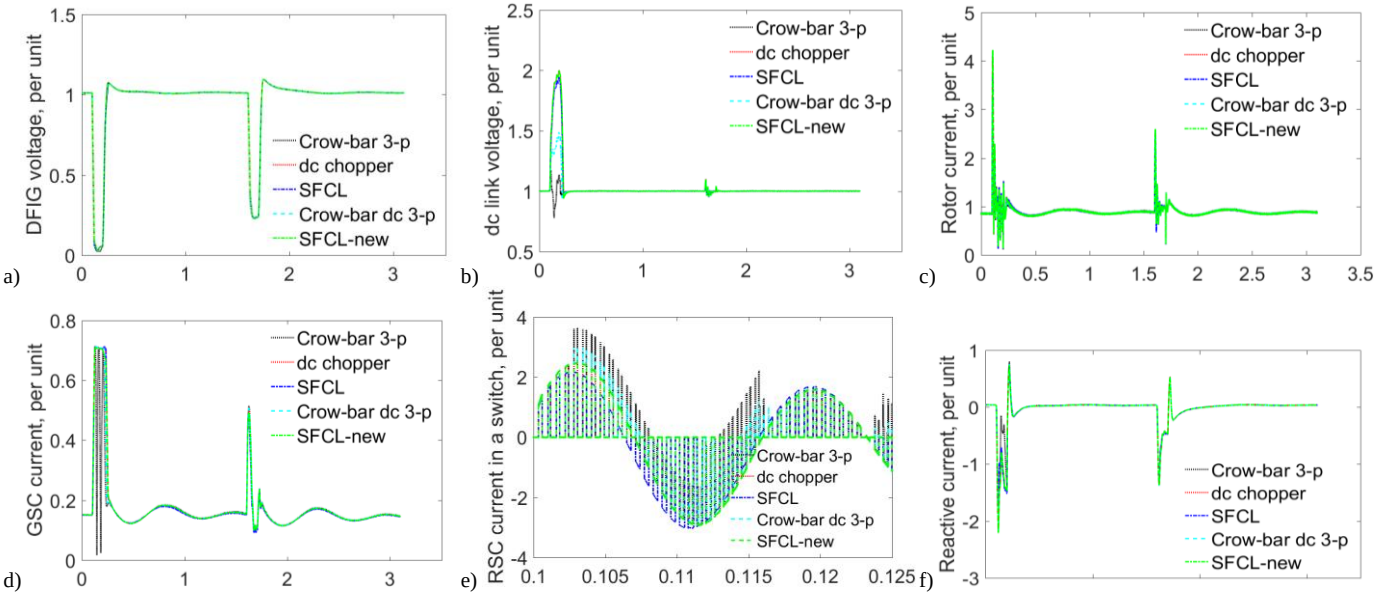
The currents of the induction machine rotor, and the RSC are analysed during the two faults. The machine rotor current is not highly affected by the disconnection of the RSC, because the machine turns to be a conventional squirrel cage induction generator, where the rotor windings are almost short-circuited. The RSC currents are displayed in sinusoidal form to reflect its evolution during the fault as shown in Figure 4(e). Compared to increase in the DC link voltage, the rotor current overshoot is almost double but in the same rate, hence the sensing method does not play a key role. The DC chopper and the SFCL achieve slight improvement in the current profile, as it is decaying faster and its peak is mitigated. The 3-phase AC crowbar caused steep oscillations in the Grid Side Converter (GSC) current, which are not visible in the other LVRT methods as shown in Figure 4(d).

Reactive compensation

The reactive current and power provision is investigated on different levels, at PCC, DFIG i.e. bus B2, and the terminals of the GSC. The reactive power suffers a natural overshoot due to the implemented DFIG conventional i_d and i_q control, before it decays very rapidly to zero due to the voltage drop as shown Figure 4(g). The reactive current reflects the same observation as shown in Figure 4(e) and (f) in both Scenarios. The reactive current is negative according to the model setup where the negative sign indicates 'generation', while positive is 'consumption'. It is of note that, the current reaches about 1.5 per unit naturally during the fault (apart from the very early overshoot at the fault start), which is healthy to the power system as it contributes to voltage dip mitigation and fast voltage recovery.

Mechanical response and stator flux evolution

The transients of the WTG pitch angle and rotor speed are not highly affected due to the very short time-scale of voltage events compared to the mechanical interactions in a WTG, considering its inertia, and the mechanical delay of the pitch angle. Thus, the impact of the applied fault-sensing and LVRT methods is minor as shown in Figure 4(i) and Figure 5(a). Likewise, the evolution of the magnitude of *d* and *q* components of the stator flux is trivially affected by the applied sensing and LVRT method as shown in Figure 5(b).



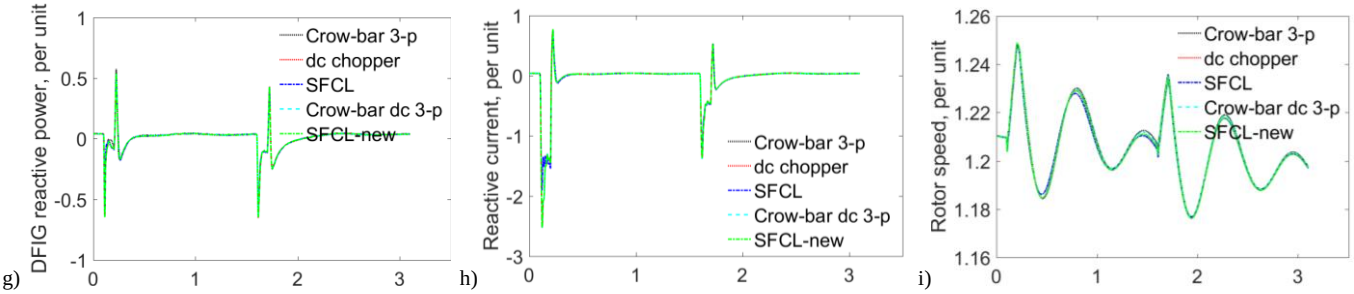


Figure 4. Scenario 1: a) voltage at DC link, b) voltage at WTG bus, c) rotor current, d) current in one of the RSC switches, and e) the GSC, f) reactive current; Scenario 2: DFIG g) reactive power, h) reactive current, i) WTG rotor speed. (3-p: 3 phase)

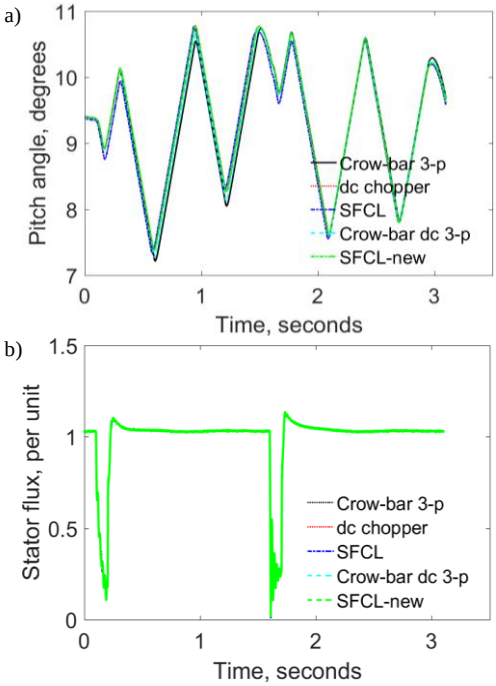


Figure 5. a) pitch angel and b) flux evolution in Scenario 2.

4 DC multi-terminal grid

This section considers different bottleneck scenarios, which can face the operation and control of a MT-HVDC from voltage stability viewpoint. The default control methods and set-points of each converter station at each AC area or WF are in Table 3. The converters connected to the AC areas are equipped with three ride through modes (only one to be operational for a given case study): voltage, droop and reactive power, and according to prior studies, the droop mode is the most convenient for MT-HVDC networks [14].

4.1 Test system and scenarios

The Cigre benchmark model [15] is modified in this paper where one of the AC grids is replaced by a SG of an equivalent aggregate capacity and a lumped load at Cb-A1 as shown in Figure 6 to provide insights on the response of synchronous machines when connected to MT-HVDC, including the detailed models of governor, exciter, etc. The conventional LVRT methods integrated to the converter stations of the five AC networks (i.e. 3 AC grids and 2 WFs) are examined at different fault conditions and locations. The applied scenarios exploit the responses of the different components of this pan-interconnected network to possible bottlenecks. Moreover, it reveals critical weaknesses of the current practices, which can disable the converter stations to ride through voltage sags, when applied to the potential MT-HVDC networks. The scenarios are described as follows:

Scenario 1: Symmetrical 3-phase fault at Bus B1 of 0.07 + j0.07 impedance and continues for 150ms.

Scenario 2: Disturbance in the controller of the offshore converter station C2, where the reference frequency of the converter controller is suddenly changed from 1 to 1.2 per unit representing a possibility of controller malfunction. The regular 1 per unit value is recovered after 60ms.

Scenario 3: Two consecutive faults at two converter stations, first is a symmetrical 3-phase fault at Bus B1 of 0.07 + j0.07 impedance that continues for 150ms. The second fault is 1-phase with the same impedance and occurs at station C2 after 50ms from the first fault and continues for 150ms.

4.2 Results and discussion

The applied scenarios exploit severe events, which occurs at the converter stations of the MT-HVDC, and have mutual impacts on the power exchange as well as voltage stability across the DC grid. The responses at key buses, which are the most affected by the incident, are displayed and discussed. The different control modes (i.e. voltage, droop and reference reactive power) of the AC grids converters (i.e. Conv. A1, B2 and B2) are tested, where in each case all the converters adopt the same mode. The divergence between the results obtained at each mode are minor, hence the results displayed are for the widely applied mode which is droop control [14].

Scenario 1

The fault at B1 drags the voltage to almost zero, causing steep transients at the DC buses B4 and B1 as shown in Figure 7(a).

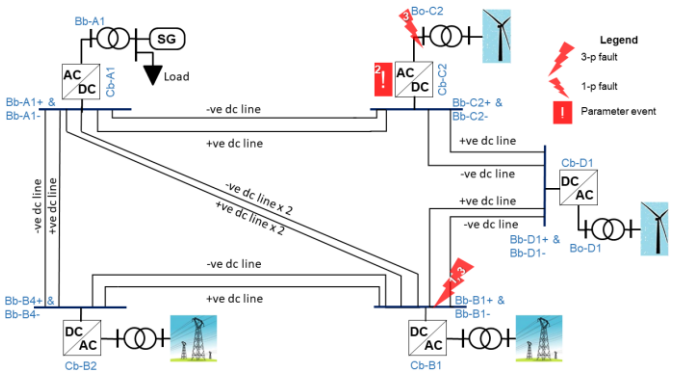


Figure 6. MT-HVDC test system (white numbers in the red logos of the events refer to scenario number)

Stations	Rating	Control method	AC/DC references	Power reference
Cb-A1 [SG]	2.4 GVA	Vac-Vdc	1/1.02	-
Cb-B1	2.4 GVA	Vac-P	1/-	1500 MW
Cb-B2	2.4 GVA	Vac-P	1/-	1500 MW
Cb-C2 [WF]	0.5 GVA	Vac-phi	1.00 (0°)/-	-
Cb-D1 [WF]	1.2 GVA	Vac-phi	1.00 (0°)/-	-

Table 3. Converter stations control methods and ratings (the value between brackets is the reference phase angle)

However, B4 is more affected, as it is still trying to exchange power with the DC grid by being directly connected to a faulted AC area, meanwhile B1, connected to the affected converter station suffers a positive voltage deviation as shown in Figure 7(a). The reactive current of the WF converter station D1 is unaffected, as it does not have direct connection to the faulted AC area. The SG, connected via converter station A1, reduces its active current as depicted in Figure 7(b), where the exported power to the faulted AC area disturbs the power balance across the DC grid, and the reactive power was also reduced as a compulsory reaction to maintain the AC voltage level.

The converter at the faulted area increases its reactive current considerably to tackle the voltage dip, besides the overshoot of the active current due to the occurring fault fed by the active power imported by the DC grid. The positive and negative DC lines connected to the DC bus of the faulted AC area are also moderately affected, especially the currents which are oscillating during the fault but with a mild amplitude of about ±10% of the actual steady state value. This also returns to the modelling parameters of the DC lines, which requires further investigations.

Scenario 2

This scenario reveals the possible risks in case of an erroneous control process at one of the converter stations. The DC voltage of the station that suffers the incident is the most affected as shown in Figure 8(a), which also reflects to the major oscillations at the AC side.

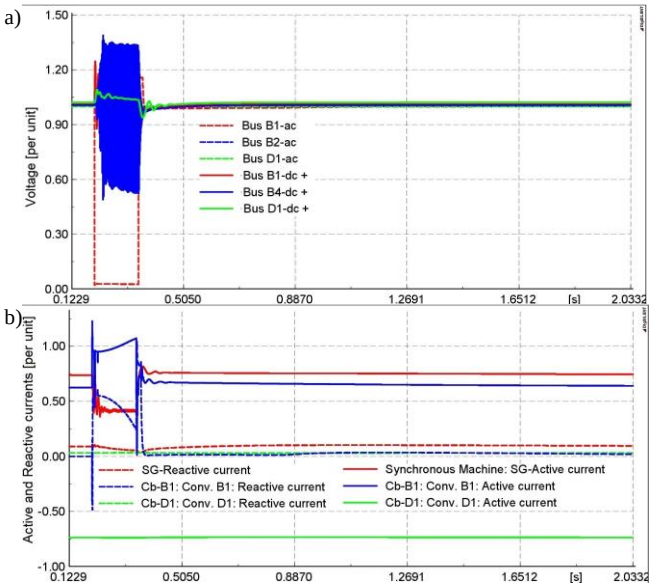


Figure 7. Scenario 2: a) voltage at key buses, b) active and reactive currents of key converter stations.

The other WF is slightly affected, meanwhile the AC areas show minor oscillations at the DC buses. The behaviour of the SG is trying to compensate the DC voltage drop, which increases the current across a part of the DC grid, hence active power consumption increases in the form of losses across the DC grid. In particular, the active current increases rapidly before it drops when the DC voltage overshoots as shown in Figure 8(b). The affected station C2, responds in a similar manner, where the active current increases, however, the reactive current drops for two reasons, first, reaching the PQ capability limitations of the converter. Second, the WF cannot export all the available power, thus the AC voltage increases so the converter tries to mitigate the voltage by reducing its reactive current compared to its steady state value. The DC voltage is much less affected, and it recovers rapidly and smoothly to the pre-event steady state conditions.

Scenario 3

The probability of occurrence of two simultaneous faults at two AC connection points within a DC grid is marginal, however, this scenario pushes the system to the limits as evident from the results obtained. The critical instability is not caused only by fault currents, but also the temporary power unbalance across the DC grid. The closer stations are brought to focus, where the voltage responses at the AC and DC buses at A1, C2 and D1 are shown in Figure 9(a).

The voltages at the DC buses are slightly affected. This ensures the reliability of the DC grid that decouples different events at the AC areas and WFs. In addition, the voltage recovery of the 1-phase fault is smoother, and caused reduced oscillations on the DC side voltage. The 1-pahse nature of the second fault enabled the converter station at C2 to provide very high reactive current to compensate the voltage drop as shown in Figure 9(b), meanwhile the active current is mitigated to comply with the PQ capability of the converter. The SG increases its output power to compensate for the power unbalance, while the reactive current is almost constant. The oscillations in the current flowing through the selected DC lines are relatively more intensive compared to the previous scenarios, mainly when the two faults overlap. The reactive power provision by the SG and the converters is analysed, where the reactive power of the healthy stations has slightly changed to accommodate the new set-points that are enforced by the events as shown in Figure 9(c). Conversely, station C2 is pushing to the limits to curtail the voltage dip, taking the advantage of suffering a 1-phase fault not a 3-phase. The SG deviates slightly from its steady state generation, as it reduces its reactive output to allow more active power production without violating the voltage stability within its AC area. It is of note that, the local load fed by the SG has a high reactive demand to examine the DC grid if the SG has a limited room to supply extra reactive power. This case could be found in real-world if the AC area is dominated by certain types of industries, which act as huge inductive loads.

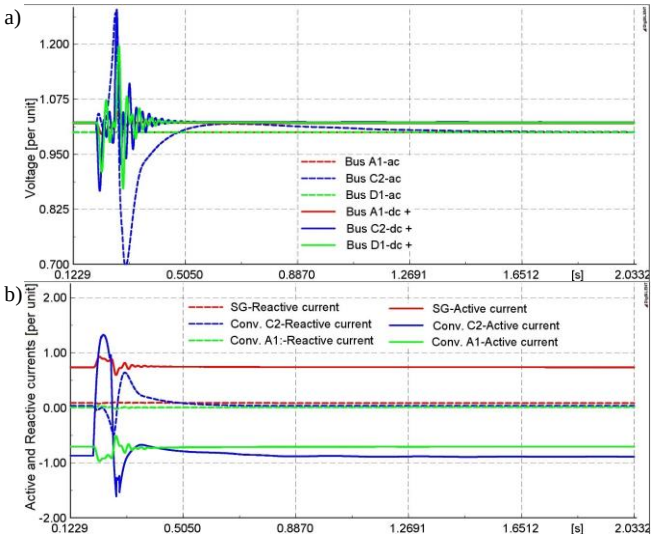


Figure 8. Scenario 2: a) Voltage at key buses, b) Active and Reactive currents of key converter stations.

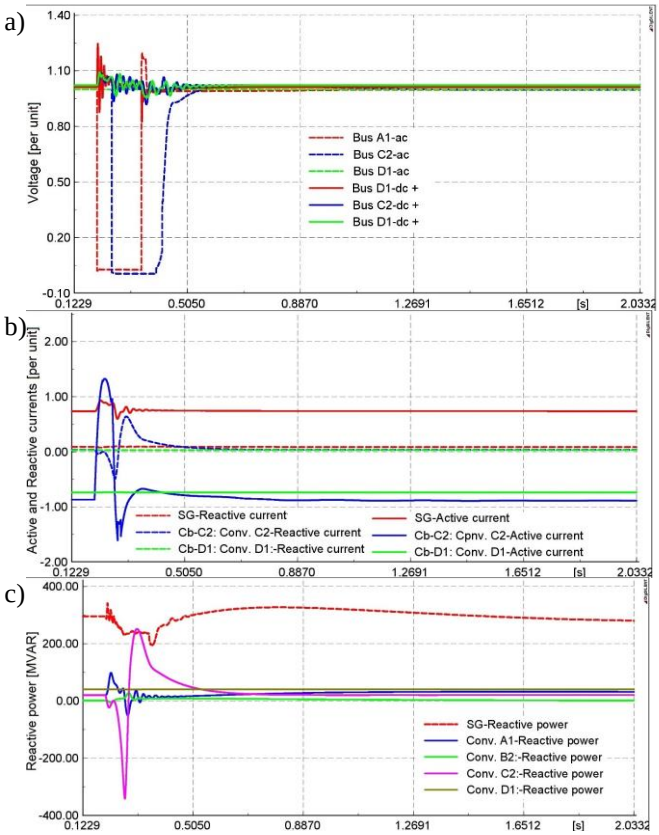


Figure 9. Scenario 3: a) voltage at key buses, b) active and reactive currents of key converter stations and c) reactive power demand/supply of the SG and 4 converter stations.

5 Conclusions

This paper provides a wide virtual demonstration on voltage stability in different systems, which are used to deliver wind power. The conventional protection hardware of Type 3 wind turbine is compared and analysed under different scenarios, in addition to the possibility of using superconductive current limiter as a responsive sensorless alternative. The results show limited diversities between the examined protection hardware as well as the sensing methods, but the conventional crowbar is always the safest option, while the SFCL shows a good potential which requires further investigations mainly on the design of the SFCL resistance. The capability of wind turbine to comply with reactive compensation requirements is limited at the early stage of the event, however, it is improved at less severe events and during voltage recovery.

Some relevant modifications are applied to Cigre benchmark DC network to examine the impact of some critical scenarios. The obtained results show the incapability of the conventional control methods to deal with some events including the loss of DC connecters, where the affected link must be shutdown and reenergised even if the drop is not very severe. The DC nature of the grid helps to isolate voltage events at AC grids, however, the power exchange across the whole DC grid is affected during faults because the faulted AC grid cannot import/export the assigned amount of power to maintain the balance between generation and demand across the DC grid. One of the key observations is the ability of the available control methods to handle unexpected control errors.

Acknowledgements

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